REMARKS

Initially, reconsideration and continued examination is respectfully requested. Applicants wish to thank the Examiner for the detailed Final Office Action and for the Notice of References Cited.

In the outstanding Final Office Action, claims 1-2 and 7-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI et al. (U.S. Patent No. 6,397,298) in view of "Modern Operating Systems, 2nd Edition" to Andrew S. TANENBAUM. Claims 3-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI et al. in view of TANENBAUM as applied to claim 2 above, and further in view of PETTEY (U.S. Patent No. 6,021,480).

Upon entry of the present amendment, independent claims 1 and 10 will have been amended, dependent claim 4 will have been cancelled and new independent claim 11 will have been added. Support for the amendments to independent claims 1 and 10 and the addition of new independent claim 11 may be found at, for example, page 11, lines 3-9 of Applicants' Application specification as filed (*i.e.*, paragraph [0096] of the published application, U.S. Patent Application Publication No. 2008/0168232) and page 18, line 32 to page 19, line 9 of Applicants' Application specification as filed (*i.e.*, paragraph [0145] of the published application). The amendments to independent claims 1 and 10, the cancellation of dependent claim 4 and the addition of new independent claim 11 should not be considered an indication of Applicants' acquiescence as to any of the outstanding rejections. Rather, Applicants have amended independent claims 1 and 10, cancelled dependent claim 4 and added new independent claim 11 solely to advance the prosecution and to obtain an early allowance of the present application.

Initially, Applicants note that the Examiner still has not indicated consideration the Information Disclosure Statement filed on September 15, 2006, which the Examiner asserts fails to comply with 37 C.F.R. §1.98(a)(1). As previously discussed, the documents cited in the Information Disclosure Statement filed on September 15, 2006 were earlier submitted for the Examiner's consideration with the Information Disclosure Statement filed on July 21, 2006 (as noted on page 2 of the Information Disclosure Statement filed on September 15, 2006) *and* the Examiner acknowledged consideration of each of the documents cited in the Information Disclosure Statement filed on July 21, 2006. Thus, unless indicated otherwise in the next Official communication, Applicants conclude that the Examiner considered the materials noted in the September 15, 2006 Information Disclosure Statement, said documents having earlier been considered in the July 21, 2006 Information Disclosure Statement.

Applicants respectfully traverse the outstanding rejections. Applicants' amended independent claim 1 recites, *inter alia,* a modifier that attaches, to the modified order data, an oldest-order flag which indicates, when enabled, that the access order is the oldest regardless of the actual access order and which indicates that the cache entry to be replaced is written to no further. Applicants independent claim 1 further recites, *inter alia,* that the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset, each cache entry being reset when a 1-bit order flag is enabled for each cache entry. Applicants' independent claim 1 also recites, *inter alia,* that said selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having the oldest-order flag enabled is present and that said selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag unenabled is present.

Applicants respectfully submit that the combination of ARIMILLI et al. and TANENBAUM as set forth by the Examiner fails to disclose or render obvious at least these claimed features of Applicants' independent claim 1.

The Examiner again relies on ARIMILLI et al. as teaching the claimed modifier and the claimed selector, and again asserts an R bit flag disclosed by TANENBAUM as teaching the claimed 1-bit order flag and an M bit flag disclosed by TANENBAUM as teaching the claimed oldest-order flag. In the *Response to Arguments* section of the outstanding Final Office Action, the Examiner asserts that the M bit flag disclosed by TANENBAUM reads on the claimed "oldest-order-flag" insofar as TANENBAUM's M bit flag can provide oldest [access] order information. The Examiner sets forth an example in which there are two cache entries with one cache entry having M=1, while the other cache entry has M=0. Thus, the Examiner asserts that the M bit acts as an "older-order flag" because the cache entry having M=1 is older in terms of when it was accessed compared to the cache entry having M=0. However, TANENBAUM is submitted to disclose a status bit M that is set when the page is written. TANENBAUM is further submitted to disclose that the M bit must be updated on every memory reference; once a bit has been set to 1 it stays set to 1 until the operating system resets it to 0 in software. *See, e.g.,* page 216, lines 14-17 of TANENBAUM. Applicants respectfully submit that TANENBAUM fails to disclose or render obvious a modifier that attaches, to the modified order data, an oldest-order flag which indicates, when enabled, *that the access order is the oldest regardless of the actual access order and which indicates that the cache entry to be replaced is written to no further*.

According to a non-limiting aspect of the presently claimed invention, a weak flag W is a flag that specifies that the access order of a cache entry is regarded as the oldest. That is, W=1 means that the processor 1 reads out and writes to the cache entry no further, or that an access

frequency is low. Furthermore, W=1 indicates that the access order regarding a replace control is treated as the oldest, or in other words, that it is a weakest (weak) cache entry, and W=0 indicates that such is not the case. *See, e.g.,* page 11, lines 3-9 of Applicants' Application specification as filed (*i.e.,* paragraph [0096] of the published application). TANENBAUM is submitted to merely disclose *a status bit M that is set when a page is written*. Applicants respectfully submit that TANENBAUM fails to disclose that the M bit indicates that an access order is the oldest, *irrespective of an actual access order*. Applicants further submit that the M bit disclosed by TANENBAUM does not indicate that *a cache entry to be replaced is written to no further*.

TANENBAUM is also submitted to disclose a status bit R that is set whenever a page is referenced (read or written) and that periodically, (*e.g.,* on each clock interrupt), the R bit is cleared, to distinguish between pages that have not been referenced recently from those pages that have been recently referenced. *See e.g.,* page 216, lines 27-29 of TANENBAUM. TANENBAUM is further submitted to disclose that the R bit must be updated on every memory reference; once a bit has been set to 1 it stays set to 1 until the operating system resets it to 0 in software. *See, e.g.,* page 216, lines 14-17 of TANENBAUM. However, Applicants' amended independent claim 1 recites, *inter alia,* that the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset, *each cache entry being reset when a 1-bit order flag is enabled for each cache entry*. It is submitted that TANENBAUM merely discloses R bits are cleared on each clock interrupt, and not when all of the 1-bit order flags for each of the cache entries are enabled (*i.e.,* set to "1"), as specified in Applicants' independent claim 1.

According to another non-limiting aspect of the presently claimed invention, a use flag U indicates whether a cache entry has been accessed, and is used at the time of a replacement due to a mishit in a least recently used (LRU) method, in place of the access order data in the cache

entries of the four ways. More particularly, a use flag U of 1 indicates that an access has occurred, and 0 indicates that no access has occurred. That is, the use flag indicates two relative states, whether the time of access is old, or new. In other words, the cache entry with a use flag of 1 has been accessed more recently than a cache entry of a use flag of 0. *When all use flags of the four ways in one set because 1, the use flags are reset to 0. See, e.g.,* page 18, line 32 to page 19, line 9 of Applicants' Application specification as filed (*i.e.,* paragraph [0145] of the published application).

At least insofar as ARIMILLI et al. in view of TANENBAUM fails to disclose or render obvious either the claimed oldest-order flag or the claimed 1-bit order flag, Applicants respectfully submit that the combination of ARIMILLI et al. in view of TANENBAUM fails to disclose or render obvious a selector that selects the cache entry to be replaced when a cache miss occurs and a cache entry having the oldest-order flag enabled is present and that said selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag unenabled is present. That is, Applicants' independent claim 1 specifies choosing an order based on whether an oldest-order flag is enabled.

With regard to the features previously recited in now-cancelled dependent claim 4 and now substantially recited in Applicants' amended independent claim 1, the Examiner asserts column 4, lines 61-65 and column 3, lines 36-37 and FIG. 1, element 15 of ARIMILLI et al. and the M bit disclosed by TANENBAUM. In this regard, ARIMILLI et al. is submitted to disclose a cache memory 16 for storing a subset of information (*i.e.,* instructions and/or data) that are stored within main memory 12. ARIMILLI et al. is further submitted to disclose that an access status of the cache line after the linefill operation can be assigned to any access status, and that the access

status is preferably assigned to an access status other than the most recently used (MRU) status (*i.e.*, MRU-1 status through least recently used (LRU) status). However, both ARIMILLI et al. and TANENBAUM fail to disclose or render obvious at least a modifier that attaches, to the modified order data, an oldest-order flag which indicates, when enabled, that the access order is the oldest regardless of the actual access order and which indicates *that the cache entry to be replaced is written to no further*, as recited in Applicants' independent claim 1. In fact, ARIMILLI et al. teaches away from these features recited in Applicants' independent claim 1 insofar as ARIMILLI et al. is submitted to disclose that the cache line may be subsequently accessed or referenced after assigning the access status other than the MRU status. *See, e.g.,* column 4 line 66 through column 5, line 6 of ARIMILLI et al. Further, even assuming, *arguendo,* that ARIMILLI et al. or TANENBAUM were properly interpretable as teaching the claimed oldest-order flag (and Applicants submit that neither ARIMILLI et al. nor TANENBAUM can be so interpreted), neither ARIMILLI et al. nor TANENBAUM, either singularly or in any proper combination, disclose or render obvious that a cache entry to be replaced is selected based on an access order which is chosen based on whether the claimed oldest-order flag is enabled, as specified in Applicants' independent claim 1.

In view of the above, Applicants respectfully submit that independent claim 1 is allowable over ARIMILLI in view of PALANCA for at least the reasons set forth above.

In addition, the method of independent claim 10 is submitted to be allowable for reasons similar to those noted above with respect to independent claim 1 in addition to reasons related to its own recitations.

Applicants respectfully submit that each of dependent claims 2 and 7-9 are allowable at least because they depend, directly or indirectly, from independent claim 1 which Applicants submit has been shown to be allowable. Each of dependent claims 2 and 7-9 are also believed to

recite further patentable subject matter. Applicants submit that the cancellation of dependent claim 4 renders moot the rejection of dependent claim 4 over ARIMILLI et al. in view of TANENBAUM and PETTEY. Further, arguments made above with respect to the rejection of independent claim 1 are applicable hereto insofar as claim 3 depends from independent claim 1. Applicants respectfully submit that dependent claim 3 is also believed to recite further patentable subject matter and that PETTEY fails to cure the deficiencies noted above with respect to the combination of ARIMILLI et al. in view of TANENBAUM set forth by the Examiner. As such, allowance of the dependent claims is deemed proper for at least the same reasons noted for the independent claims upon which they depend, in addition to reasons related to their own recitations.

New independent claim 11 is submitted for the Examiner consideration. In this regard, Applicants submit that none of ARIMILLI et al., TANENBAUM and PETTEY, either singularly or in any proper combination, discloses or renders obvious the claimed combination of features recited in new claim 11.

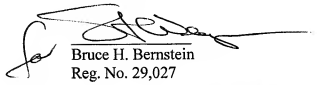
In view of the above, reconsideration and withdrawal of the rejection of claims 1, 2 and 7-10 under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI in view of PALANCA and the rejection of claims 3 and 4 under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI in view of PALANCA as applied to claim 2 above, and further in view of PETTEY is respectfully requested.

At least in view of the herein contained amendments and remarks, Applicants respectfully request reconsideration and withdrawal of each of the outstanding rejections, together with an indication of the allowability of all pending claims, in due course. Such action is respectfully requested and is believed to be appropriate and proper.

Should an extension of time be necessary, the Commissioner is hereby authorized to charge any additional fee to Deposit Account No. 19-0089.

Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully Submitted,
Hazuki OKABAYASHI et al.



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August 24, 2010
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